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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,060	02/04/2004	Gaku Minamihara	04329.3238	2231

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EXAMINER	
GOODWIN, DAVID J	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,060	MINAMIHARA ET AL.	
	Examiner	Art Unit	
	David Goodwin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/12/06, 2/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimagaki (US 6,953,388) in view of Burke (US 2002/0098789 A1).

3. Regarding claim 11.

4. Shimagaki teaches a method of polishing a substrate. Said method comprises a pad for use in CMP (column 1 lines 5-15). The polishing process is used on insulating or metallic layers formed on a semiconductor wafer (column 19 lines 20-30). The process comprises. The polishing process uses a polishing slurry (column 13 lines 45-55). Polishing slurries are applied to the surface of the substrate. The pad comprises a resin matrix (column 5 lines 20-35). Further the pad comprises particles of soluble material that will elute out during the polishing process forming interstices in the surface of the pad (column 13 lines 40-60). The amount of soluble material is preferably between 0.5 and 5.0 wt% (column 14 lines 1-5). The material for the polishing pad matrix and the soluble particles have a density of approximately 1 g/cm^3 and will therefore result in a soluble particle volume component ranging from 0.5 to 5.0 % of the pad total volume.

5. Shimagaki does not teach the size of the eluting particles.

6. Burke teaches a method of making a semiconductor device. Said method comprising a polishing pad being used to apply abrasive slurries to the substrate (paragraph 34). Said pad comprising a matrix (11) having cells (14) recessed into the matrix (11) dispersed across a surface region of the polishing pad (fig 3) (paragraph 36). Each cell is formed by the liberation of a particle from the matrix leaving a void with a size ranging from 5 to 250 microns (paragraph 51) thereby forming a surface having a microtexture of 1-5 microns (paragraph 35).

7. It would have been obvious to one of ordinary skill in the art to use particles of 5 to 250 microns in order to transfer sufficient slurry across the surface of the substrate.

8. Regarding claim 19.

9. Shimagaki teaches that the polishing slurry may contain abrasive grains (column 13 lines 55-65).

10. Regarding claim 20.

11. Further the pad comprises particles of water soluble material that will elute out during the polishing process forming interstices in the surface of the pad (column 13 lines 40-60).

12. Claims 12 through 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimagaki (US 6,953,388) in view of Burke (PG Pub 2002/0098789 A1) and further in view of You (US 6,663,787 B1).

13. Regarding claim 12.

14. Shimagaki in view of Burke does not teach that the polishing pad may be used to polish a conductive layer formed over an insulating layer.

15. You teaches a method of making a semiconductor device using a copper damascene method. Said method comprising depositing a first insulating layer (142) forming a second insulating layer (113) over the first insulating layer (142) (fig 5d) (column 18 lines 15-45). Forming a recess (146) in the insulating layers (fig 5g) (column 19 lines 10-30). Deposing a conductive layer (122) over the insulating layers (fig 5k) (column 20 lines 20-40). Polishing the conductive layer to form a wiring layer (fig 5L) (column 20 lines 40-55).

16. It would have been obvious to use the polishing pad and process of Burke to polish the conductive layer of You in order to get a highly planar surface.

17. Regarding claim 13.

18. You further teaches the use of copper as the conductive layer to be polished (column 20 lines 20-40).

19. It would have been obvious to use copper as the conductive layer in order to get a highly conductive metallization.

20. Regarding claims 14, 15, and 16.

21. You further teaches the use of silicon nitride as the second layer (column 18 lines 50-60) and polyaryl ether as the first layer (column 18 lines 5-10). Polyaryl ether has a dielectric constant of less then 2.5 and silicon nitride has a dielectric constant higher then polyaryl ether.

22. It would have been obvious to one of ordinary skill in the art to use silicon nitride over polyaryl ether in order to minimize the intermetal insulator dielectric constant and protect the low dielectric constant intermetal dielectric from polishing damage.

23. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimagaki (US 6,953,388) in view of Burke (PG Pub 2002/0098789 A1) and further in view of Jang (US 5,702,977).

24. Shimagaki in view of Burke teaches all elements of the claimed invention above.

25. Shimagaki in view of Burke does not teach the use of the polishing to polish an insulator deposited in a trench.

26. Jang teaches a method of making a semiconductor device. Said method comprises providing a semiconductor substrate (30) (column 5 lines 45-55). Forming a trench (29) in the semiconductor (30) (fig 3) (column 5 lines 50-65). Depositing an insulating layer (42) over the trench (29) and substrate (30) (column 9 lines 45-55). Polishing the insulating layer to form a patterned buried insulating region (42b) (fig 8) (column 10 lines 30-45).

27. It would have been obvious to use the polishing pad and process of Burke to polish the insulating layer of Jang in order to get a highly planar surface.

28. Regarding claim 18.

29. Jang teaches that the insulating layer (42) comprises silicon dioxide (column 9 lines 55-65).

30. It would have been obvious to one of ordinary skill in the art to use silicon dioxide for the insulating layer formed in the trench because it provides adequate isolation in an efficient process.

Response to Arguments

31. Applicant's arguments with respect to claims 11 through 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Goodwin whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJG

David Nelms
Supervisory Patent Examiner
Technology Center 2800